Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in this application.

Listing of the Claims:

1. (currently amended) An IC card supplied with an operating voltage by an electrical connection between each of external terminals and a read/write device, and including an input-output operation of data with an encoding process or a decoding process being executed by an encoding processing computing unit operated in response to instructions issued from a central processing unit, and further using random numbers generated by a random number generator as pseudo address signals to transfer data to the encoding processing computing unit,

~~wherein~~ said encoding processing computing unit ~~is provided with each of~~ including registers, which ~~stores~~ store data used for a computation for the encoding process or the decoding process ~~in plural bit units, and data necessary~~ prior to performing the encoding process or the decoding ~~process is stored in the register~~ process, and

wherein said registers further store calculated results from the computation for the encoding process or the decoding process.

2. (currently amended) The IC card according to claim 1, wherein said encoding process or decoding process includes an exponential residue multiplying operation ~~applicable to RSA cryptography or the like~~, and

said encoding processing computing unit alternately computes $A=A^2$ mod N and A=AB mod N with A=1 and B=X in response to X, Y and N ~~inputted~~ being input thereto~~,~~ ~~computes $A=A^2$ mod N corresponding to plural bits as viewed by plural~~ for each of a plurality of bits in Y starting from a high order bit of Y ~~upon said computation~~, and ~~brings~~ the value of B ~~necessary for the computation of AB mod N~~ being read from the ~~register in association with combinations of the plural bits~~ registers.

3. (currently amended) An IC card supplied with an operating voltage by an electrical connection between each of external terminals and a read/write device, and including an input-output operation of data with an encoding process or a decoding process being executed by an encoding processing computing unit operated in response to instructions issued from a central processing unit, and further using random numbers generated by a random number generator as pseudo address signals to transfer data to the encoding processing computing unit,

~~wherein~~ said encoding processing computing unit [[has]] including a signal path [[for]] and capturing

data to be used for [[the]] a next computation from a storage circuit concurrently with a computing operation for the encoding process or the decoding process via said signal path.

4. (currently amended) The IC card according to claim 3, wherein [[said]] the encoding process or the decoding ~~encoding~~ process includes an exponential residue multiplying operation ~~applicable to RSA cryptography or the like~~, and

said encoding processing computing unit alternately computes $A=A^2$ mod N and A=AB mod N with [[A-1]] A=1 and B=X in response to X, Y and N ~~inputted~~ being input thereto, ~~computes $A=A^2$ mod N corresponding to plural bits as viewed by plural~~ for each of a plurality of bits in Y starting from a high order bit of Y ~~upon said computation~~, and ~~brings~~ the value of B being read ~~necessary for the computation of AB mod N corresponding to combinations of the plural bits~~ from the storage circuit concurrently with said computation of A^2 mod N.

5. (currently amended) An IC card, which is supplied with an operating voltage by an electrical connection between each of external terminals and a read/write device, ~~in which~~ the IC card comprising:

a central processing unit, a storage circuit, an encoding processing computing unit and a random number

generator ~~are~~ each connected to a common address bus[[,]] ; ~~and which includes~~

wherein an input-output operation of data with an encoding process or a decoding process is executed by the encoding processing computing unit and the storage circuit operated in response to instructions given from the central processing unit,

wherein said central processing unit supplies a leading address at which data for the encoding process or the decoding process is stored, to the storage circuit, and [[said]] the storage circuit reads the data, based on an address signal formed by a built-in address generating circuit based on the leading address and transfers the [[same]] data to the encoding processing computing unit, and each of a plurality of random numbers produced by the random number generator is transmitted to an address bus commonly connected with the central processing unit, the storage circuit and the encoding processing computing unit as a pseudo address signal in association with the data transfer.

6. (currently amended) The IC card according to claim 5, wherein [[said]] the encoding process or the decoding process includes an exponential residue multiplying operation ~~applicable to RSA cryptography or the like~~, and

said encoding processing computing unit alternately computes $A=A^2$ mod N and A=AB mod N with A=1 and B=X in response to X, Y and N ~~inputted~~ being input thereto, ~~computes $A=A^2$ mod N corresponding to plural bits as viewed by plural~~ for each of a plurality of bits in Y starting from a high order bit of Y ~~upon said computation~~, and ~~brings~~ the value of B ~~necessary for the computation of AB mod N~~ being read from the storage circuit in association with combinations of the ~~plural~~ plurality of bits.

7. (currently amended) An IC card, which is supplied with an operating voltage by an electrical connection between each of external terminals and a read/write device, ~~in which~~ the IC card comprising:

a central processing unit, a storage circuit, an encoding processing computing unit and a random number generator [[are]] each connected to a common address bus[[,]]; ~~and which includes~~

wherein an input-output operation of data with an encoding process or a decoding process is executed by the encoding processing computing unit and the storage circuit operated in response to instructions given from the central processing unit,

~~wherein~~ said central processing unit supplies an encoded address signal formed using each of a plurality of random numbers produced by the random number generator

to the storage circuit, which decodes the address signal through the use of the random number to generate a leading address,

said storage circuit reads data for the encoding process or the decoding process, based on the address signal produced by a built-in address generating circuit on the basis of the leading address and transfers the [[same]] data to the encoding processing computing unit, and

each of the plurality of random numbers produced by the random number generator is transmitted to the address bus that is commonly connected with the central processing unit, the storage circuit and the encoding processing computing unit as a pseudo address signal in association with the data transfer.

8. (currently amended) The IC card according to claim 7, wherein said encoding process or decoding process includes an exponential residue multiplying operation ~~applicable to RSA cryptography or the like~~, and

said encoding processing computing unit alternately computes $A=A^2$ mod N and A=AB mod N with A=1 and B=X in response to X, Y and N ~~inputted~~ being input thereto, ~~computes $A=A^2$ mod N corresponding to plural bits as viewed by plural~~ for each of a plurality of bits in Y starting from a high order bit of Y ~~upon said~~

~~computation~~, and ~~brings~~ the value of B being read from the storage circuit in association with combinations of the ~~plural~~ plurality of bits.

9. (currently amended) A microcomputer having a module configuration including [[a]] an input-output operation of data with an encoding process or a decoding process executed by an encoding processing computing unit operated in response to instructions given from a central processing unit, and further using random numbers generated by a random number generator as pseudo address signals to transfer data to the encoding processing computing unit,

~~wherein~~ said encoding processing computing unit ~~is provided with each of~~ including registers, which ~~stores~~ store data used for a computation for the encoding process or the decoding process ~~in plural bit units, and data necessary~~ prior to performing the encoding process or the decoding process ~~is stored in the register~~,

said registers to store calculated results from the computation for the encoding process or the decoding process.

10. (original) The microcomputer according to claim 9, wherein said module configuration is formed on one semiconductor substrate for the implementation thereof.

11. (currently amended) A microcomputer having a module configuration, ~~including~~ and an input-output operation of data with an encoding process or a decoding process executed by an encoding processing computation unit operated in response to instructions issued from a central processing unit, and further using random numbers generated by a random number generator as pseudo address signals to transfer data to the encoding processing computing unit,

~~wherein~~ said encoding processing computing unit [[has]] including a signal path [[for]] and capturing data used for the next computation from a storage circuit concurrently with a computing operation for the encoding process or the decoding process via said signal path.

12. (currently amended) A microcomputer having a module configuration in which a central processing unit, a storage circuit, an encoding processing computing unit and a random number generator are each connected to a common address bus[[,]]; ~~and which includes~~

wherein an input-output operation of data with an encoding process or a decoding process is executed by the encoding processing computing unit and the storage circuit operated in response to instructions given from the central processing unit,

~~wherein~~ said central processing unit supplies a leading address at which data for the encoding or the decoding process is stored, to the storage circuit,

said storage circuit reads data, based on an address signal formed by a built-in address generating circuit based on the leading address and transfers the data to the encoding processing computing unit, and

said random number generator transmits each of a plurality of produced random numbers to an address bus that is commonly connected with the central processing unit, the storage circuit and the encoding processing computing unit as a pseudo address signal in association with the data transfer.

13. (currently amended) A microcomputer having a module configuration in which a central processing unit, a storage circuit, an encoding processing computing unit and a random number generator are each connected to a common address bus[[,]]; and which has ~~includes~~ an input-output operation of data with an encoding process or a decoding process executed by the encoding processing computing unit and the storage circuit operated in response to instructions given from the central processing unit,

wherein said central processing unit supplies an encoding address signal formed using each of a

plurality of random numbers produced by the random number generator, to the storage circuit,

said storage circuit decodes the encoded address signal supplied from the central processing unit by using the random number to thereby generate a leading address, reads data for the encoding or decoding process and transfers the data to the encoding processing computing unit, and

said random number ~~circuit~~ generator transmits each of the plurality of [[the]] produced random ~~number~~ numbers to the address bus that is commonly connected with the central processing unit, the storage circuit and the encoding processing computing unit as a pseudo address signal in association with the data transfer.